REMARKS

Reconsideration of the application is respectfully requested.

The Examiner's communication dated Feb. 15, 2006, which includes final rejection, is acknowledged. The present response is necessitated by new grounds for rejection in the final office action.

Claims 1 – 6, 8 – 33 and 36 – 59 are pending, and claims 2, 12 – 15, 17 – 25, 36, 37, 42 – 46, and 50 – 54 remain withdrawn from consideration under the restriction requirements. Claims 4, 26 – 33, 38 – 41, 47 – 49, and 55 – 57 stand rejected under 35 USC § 112. Claims 1, 3, 11, 16, and 58 – 59 stand rejected as anticipated under 35 USC § 102. Claims 4 – 6, 8 – 10, 26 – 33, 38 – 41, 47 – 49, and 55 – 59 stand rejected for obviousness under 35 USC § 103. No changes to these claims are made by this response.

Rejections under 35 USC § 112 traversed

Claim 4 stands rejected under 35 USC § 112, first paragraph. This rejection is respectfully traversed. There is no requirement in 35 USC § 112 or in any of the law or rules that a feature of a claim be shown in any particular figure such as a figure that the Examiner used to characterize an elected embodiment (in this instance, FIG. 3). Claim 4 recites "The memory array of claim 1, wherein the silicon-rich insulator of each memory cell is electrically isolated from the silicon-rich insulators of all other memory cells." Support for the limitation of claim 4 that each memory cell is isolated from the silicon-rich insulators of all other memory cells is found in the specification as filed, at page 6 lines 23 – 29 (last ten lines of paragraph **[0031]** of the published application, US 2005/0167787 A1), which describes clearly how the isolation is accomplished. Furthermore, the isolation of silicon-rich insulator **60** by insulator **120** is clearly shown in FIG. 2 as filed. Thus, applicants have fulfilled the requirements of 35 USC § 112 for claim 4. Therefore, withdrawal of the rejection of claim 4 under 35 USC § 112 is respectfully requested.

Claims 26 – 33, 38 – 41, 47 – 49, and 55 – 57 stand rejected under 35 USC § 112, second paragraph. These rejections are respectfully traversed. With respect to claims 30, 47, and 55, the Examiner questions how two elements can be partially aligned. Applicants respectfully submit that there is nothing unclear about partial alignment in a claim limitation. As evidence that such a limitation is a known term in the art, applicants note that many issued U.S. patents in the semiconductor field and other similar fields have elements claimed as being "at least partially aligned." Applicants respectfully submit that those skilled in the art would recognize that two elements are at least partially aligned when they are aligned to some extent, but not necessarily completely aligned, e.g., when one element overlays another element to some extent but leaves a portion not overlaid. Examples of alignment that meet the limitation requirement of being "at least partially aligned" are shown in FIGS. 2, 3, 4, 6, and 7 as filed. These drawings show a preferred degree of alignment, thereby also meeting the requirement of disclosing the best mode for realizing the invention.

The Examiner also states that the structural relationships among the storage layer, the layer of silicon-rich insulator, and the memory cell are unclear. Applicants respectfully submit that each of claims 26, 38, 47, and 55 as previously amended clearly states a series of fabrication steps. If the claimed steps are performed by a person skilled in the art, the structures formed will be the structural embodiments shown in the drawings or their equivalents (applicants' specification as filed at page 15 line 1 through page 18 line 23, i.e. paragraphs **[0055]** – **[0064]** of the published application, and FIGS. 2 – 8 and 16 as filed). FIGS. 2 – 8 clearly show the structural relationships. Thus, again, applicants have fulfilled the requirements of 35 USC § 112. Therefore, withdrawal of the rejections under 35 USC § 112 and allowance of claims 4, 26 – 33, 38 – 41, 47 – 49, and 55 – 57 are respectfully requested.

Rejections under 35 USC § 102 traversed

Claims 1, 3, 11, 16, and 58 – 59 stand rejected under 35 USC § 102(b) as anticipated by Lancaster et al. (US Pat. No. 5,656,837). These rejections are respectfully traversed.

Claim 1 as previously amended recites (emphasis added):

"A memory array comprising:

a) a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors being arranged to cross at cross-points, and

b) a *two-terminal* memory cell disposed at each cross-point, each memory cell having a storage element and a control element coupled in series between a row conductor and a column conductor, and each control element including a silicon-rich insulator."

Similarly, claim 16 as previously amended recites (emphasis added):

"A memory array comprising:

a) a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors being arranged to cross at cross-points, and

b) a *two-terminal* memory cell disposed at each cross-point, each memory cell comprising means for storing data and means for controlling the means for storing data, the means for storing data and means for controlling being coupled in series between a row conductor and a column conductor, and each means for controlling including a silicon-rich insulator."

To the person of ordinary skill, the two-terminal limitation clearly means only two terminals, not at least two terminals; i.e. three- or four-terminal memory cells are not within the scopes of claims 1 or 16.

Claims 1 and 16 as previously amended clearly state the limitation to two terminals (shown in FIG. 3, in which the two terminals comprise row conductor **30** and column conductor **40**, in FIGS. 14 and 15 as filed, and in

the specification as filed at page 9 lines 3 –11 and at page 13 lines 7 – 31 (paragraphs **[0039]**, **[0051]**, and **[0052]** of the published application, US 2005/0167787 A1). Dependent claims 3, 11, 58 and 59 share the same two-terminal limitation.

The patent of Lancaster et al., on the other hand, clearly does not disclose a two-terminal memory cell. FIG. 1 of Lancaster et al. clearly shows a single memory cell **10**, formed by an FET transistor, which is well-known to be at least a three-terminal device, having source, drain, and gate. In the flash-memory-array disclosure of Lancaster et al., the substrate is employed as a fourth terminal or "node" (col. 6 lines 34 – 41, Table 1, and FIGS. 1 and 2). In the embodiments shown in Lancaster et al., FIGS. 8 –13, elements **160** and **166** are not two terminals of a two-terminal memory cell as characterized by the Examiner in this rejection. All the terminals of those cells are the same as for the embodiment of Lancaster's FIGS. 1 and 2 (Lancaster et al., col. 12 lines 59 – 62, where Lancaster et al. recite "A topographical plan view of a portion of another embodiment of a structure of a cell array **150** that has an equivalent electrical schematic diagram represented by the circuit of FIG. 2 is shown in FIG. 8." FIGS. 1 and 2 both clearly show that each memory cell of Lancaster et al. has more than two terminals. Besides the two terminals **160** and **166** identified by the Examiner, the employment of additional terminals (**154, 155** and substrate **152**), is described at col. 13 lines 44 – 65, for example. Applicants respectfully reiterate that removal of any one or two of the terminals (source, drain, gate, or substrate) of the memory cells of Lancaster et al. would render their memory cells inoperative. Therefore, the memory cells of Lancaster et al. cannot be two-terminal devices.

Thus, applicants respectfully submit that the "two-terminal" limitation clearly distinguishes claims 1, 3, 11, 16, and 58 – 59 from Lancaster et al. (US Pat. No. 5,656,837). Therefore, withdrawal of the rejections of these claims under 35 USC § 102 is respectfully requested.

Rejections under 35 USC § 103 traversed

Claims 4 – 6, 8 – 10, 26 – 33, 38 – 41, 47 – 49, and 55 – 59 stand rejected under 35 USC § 103 as being unpatentable over Lancaster et al. (US Pat. No. 5,656,837). Applicants respectfully traverse these rejections as being insufficiently supported by evidence in the record. The Examiner states that although he did not provide any evidence of obviousness in the earlier office action, the obviousness was established by using the knowledge generally available to one of ordinary skill in the art. The cases cited by the Examiner are acknowledged. However, again the Examiner has not provided a *prima facie* case of obviousness under 35 USC § 103 and in accordance with the MPEP.

Regarding claim 4, the Examiner states again that it would have been obvious "to use a silicon-rich insulator of each memory cell being electrically isolated from the silicon-rich insulators of all other memory cells in Lancaster et al.'s device in order to use the device in an application which requires various types of storage elements." Applicants respectfully submit that "use of various types of storage elements" fails to relate to the person of ordinary skill anything about isolation of silicon-rich insulators; there is simply no connection. Such a statement of motivation by the Examiner clearly does not meet the requirements of MPEP 706.02(j) and MPEP 2143 – 2144. Specifically, MPEP 706.02(j) requires that the reference(s) must teach or suggest all the claim limitations (*In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438, Fed. Circ. 1991). In the present instance, none of the references of record teaches or suggests the limitation that the silicon-rich insulator of each memory cell be electrically isolated from the silicon-rich insulators of all other memory cells.

Regarding claims 5 – 6 and 8 – 10, the Examiner again states that "it would have been obvious ... to use a control element of each memory cell comprises (sic) a tunnel junction, and the storage element of each memory cell comprises (sic) an anti-fuse, a fuse, a tunnel junction, a state-change

layer, a chalcogenide, in Lancaster et al.'s device in order to use known memory control and storage elements, of which official notice is taken." Applicants respectfully submit that "in order to use known memory control and storage elements" fails to motivate the person of ordinary skill about combinations of the specific elements claimed. Again, such a statement of motivation by the Examiner clearly does not meet the requirements of MPEP 706.02(j) and MPEP 2143 – 2144. Specifically, it is never appropriate to rely solely on "common knowledge" in the art without evidentiary support in the record, as the principle evidence upon which a rejection was based (MPEP 2144.03(A) and Zurko, 258 F.3d at 1385-86, 59 USPQ2d at 1697). In the present instance, there is no evidentiary support for the motivation of which the Examiner takes official notice.

Regarding the obviousness rejections of claims 26 – 35, 38 – 41, 47 – 49, and 55 – 57, these rejections are all predicated upon the Examiner's interpretation of FIGS. 8 –13 of Lancaster et al. as disclosing a two-terminal memory cell. As shown hereinabove, that memory cell of Lancaster et al. is cannot be a two-terminal device. Therefore, claims 26 – 35, 38 – 41, 47 – 49, and 55 – 57, all of which inherit the two-terminal limitation from a parent claim, would not be obvious in view of Lancaster et al.

For all of these reasons, applicants respectfully request that all the rejections under 35 USC § 103 be withdrawn and that claims 4 – 6, 8 – 10, 26 – 33, 38 – 41, 47 – 49, and 55 – 59 be allowed.

Applicants expressly reserve the right to file divisional and/or continuation applications with any of the canceled or non-elected claims, or with similar claims, or with claims to any subject matter disclosed in the present application or incorporated by reference.

This response is believed to be fully responsive to each issue raised in the office action, but if the Examiner maintains any rejection, applicant would

appreciate a more detailed explanation of precisely where in the references a particular combination is suggested and the relevant limitations are disclosed.

Applicants respectfully submit that the claims as previously amended are patentable over the prior art and that the application is now in condition for allowance, which is respectfully requested.

Respectfully submitted,

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